In the claims:

Please substitute the following full listing of claims for the claims as originally filed or most recently amended.

Claims 1-11 have been previously cancelled.

12. (Currently amended) An asymmetric field effect transistor comprising:

a semiconductor layer formed on an insulator layer, said semiconductor layer including impurities supplied thereto adjacent ~~at~~ edges of a trench in a dielectric layer on said semiconductor layer and adjacent source and drain regions, wherein the impurities have ~~a~~ locations precisely defined by ~~said~~ respective edges of said trench and independently tailored concentrations to produce asymmetrical diode properties at said source and drain regions for reducing floating body effects without an additional connection between said semiconductor layer between said source and drain regions and a said source region of said asymmetric field effect transistor, ~~said semiconductor layer being formed on an insulator layer,~~ and

a gate structure formed on said semiconductor layer in said trench.

13. (Previously presented) A transistor as recited in claim 12, the dielectric layer having been removed, and comprising source and drain impurity regions formed adjacent said gate structure.

14. (Previously presented) A transistor as recited in claim 13, said source and drain impurity regions having been formed by impurity implantation.

15. (Previously presented) A transistor as recited in

claim 13, including a further insulator layer deposited over said source and drain regions and said gate structure.

16. (Previously presented) A transistor as recited in claim 13, further including a further insulator layer deposited over at least said source and drain regions and planarized to said gate structure.

17. (Previously presented) A transistor as recited in claim 12, wherein said gate structure is between said source and drain regions.

18. (Previously presented) A transistor as recited in claim 17, wherein said gate structure is planarized to said dielectric layer.

19. (Previously presented) A transistor as recited in claim 12, wherein impurities were supplied by angled implantation within said trench.

20. (Previously presented) A transistor as recited in claim 12, including a sidewall within said trench.

21. (Previously presented) A transistor as recited in claim 12, wherein said impurities have been supplied by diffusion from a sidewall formed of a doped material and located in said trench.

Claim 22 (cancelled).